2244 Research Disclosure
(1995) May, No. 373, Emsworth, GB

H01L 21/4824
H01L 23/538
H01L 23/5382


XP 000518622

F p. 303-307 (compl.) = (9)

37306
Processes for Manufacturing Multilayer TAB

This disclosure provides several processes for making multilayer TAB (tape automated bonding) or flexible circuits.

I. Standard Ground Plane 2 Metal Layer Flexible Circuit Process

A process to make ground plane flexible circuits in which the first conductive layer has fine circuitry connected to a second conductive layer which functions as a ground plane for improvements in electrical properties of the circuit. The process is comprised of the steps of:

1. Sputtering a polyimide film with a seed layer of chrome and copper.
2. Plating a flash copper layer on said seed layer.
3. Laminating said photoresist on both sides of said plated film using standard laminating technique with hot rollers.
4. Exposing said photoresist on both sides to ultraviolet light through a photomask, cross linking the exposed portions of the resist.
5. Developing the unexposed portions of the resist with mild caustic solution. Normal rinsing with D. I. water and or microetching is also included in this step.
6. Plating copper side of the laminate to desired circuit thickness. This is the first conductive circuitry layer.
7. Etching of portions of polyimide film not covered by said resist by spraying or immersing the laminate into a bath of concentrated base.
8. Etching of said chrome layer by spraying or immersing with potassium permanganate/potassium hydroxide solution. This etching exposes certain areas of the circuit on 1st copper layer at the bottom of holes in polyimide film.
9. Stripping of said resist on both sides of the laminate in 2-5% solution of potassium or sodium hydroxide.
10. Cleaning of the article with normal cleaning solution, e.g., hydrogen peroxide-sulfuric acid.
11. Baking of the article in hot oven to remove all absorbed water.
12. Sputtering said article with 2nd seed layer of chrome and copper on polyimide film side.
13. Laminating said photoresist on copper side of the article to protect 1st copper layer from further

BNSDOCID: <XP____518622A__I_>

2244 Research Disclosure
(1995) May, No. 373, Emsworth, GB

plating in step #14 using standard laminating technique with hot rollers.
14) Plating said sputtered side with copper to form a second conductive layer (ground plane in this case) connected to 1st layer through vias.
15) Laminating said photoresist on said 2nd copper side using standard laminating technique with hot rollers.
16) Exposing said photoresist on both sides to ultraviolet light through a photomask, cross linking the exposed portions of the resist on said 2nd copper side and flood expose on said 1st copper side.
17) Developing the unexposed portions of the resist with above said developing sequence to open unwanted area in said 2nd copper layer. Normal rinsing with D. I. water and or microetching is also included in this step.
18) Etching of the unwanted area of said copper ground plane with said copper etchant.
19) Etching of chrome under said 2nd layer of copper using said etchant.
20) Etching of the polyimide under said unwanted copper area using said alkaline based etchant.
21) Etching of chrome under said polyimide layer vias using said etchant.
22) Stripping of resists on both sides of the article using said stripper.
23) Etching of said flash copper on lead side to produce 1st copper layer circuitry.
24) Etching of chrome under flash copper in 1st conductive layer.

II. Simplified Plated Ground Plane 2 Metal Layer Flexible Circuit Process:

The standard ground plane 2 metal layer process can be greatly simplified using additive (plating) copper for the 2nd conductive layer instead of subtractive (etching) copper. The product produced with this process will have the 2nd copper layer edge inside of the polyimide edge. For many applications, this limitation is acceptable. The process then would be comprised of the steps of:
1) Sputtering a polyimide film with a seed layer of chrome and copper.
2) Plating a flash copper layer on said seed layer.
3) Laminating said photoresist on both sides of said plated film using standard laminating technique with hot rollers.
4) Exposing said photoresist on both sides to ultraviolet light through a photomask, cross linking the exposed portions of the resist.

BNSDOCID: <XP____518622A__I_>

2244 Research Disclosure
(1995) May, No. 373, Emsworth, GB

5) Developing the unexposed portions of the resist with mild caustic solution. Normal rinsing with D. I. water and or microetching is also included in this step.
6) Plating copper side of the laminate to desired circuit thickness. This is the first conductive circuitry layer.
7) Etching of portions of polyimide film not covered by said resist by spraying or immersing the laminate into a bath of concentrated base.
8) Etching of said chrome layer by spraying or immersing with potassium permanganate/potassium hydroxide solution. This etching exposes certain areas of the circuit on 1st copper layer at the bottom of holes in the polyimide film and also in the bonding window areas and others.
9) Stripping of said resist on both sides of the laminate in 2-5% solution of potassium or sodium hydroxide.
10) Cleaning of the article with normal cleaning solution, e.g., hydrogen peroxide-sulfuric acid.
11) Baking of the article in hot oven to remove all absorbed water
12) Sputtering said article with 2nd seed layer of chrome and copper on polyimide film side.
13) Laminating said photoresist on both sides using standard laminating technique with hot rollers.
14) Exposing said photoresist on both sides to ultraviolet light through a photomask, cross linking the exposed portions of the resist on said 2nd sputtered side and flood expose on said 1st copper side.
15) Developing the unexposed portions of the resist with above said developing sequence to open area in said 2nd sputtered layer for subsequent plating of copper ground plane.
16) Plating of copper in wanted areas to form said 2nd ground plane.
17) Stripping of resists on both sides using said stripping solution.
18) Etching of flash copper on 1st conductive side and sputtered copper on 2nd conductive side using said copper etchant.
19) Etching of sputtered chrome layer both sides.

This process needs only one polyimide etching step since vias and windows were etched simultaneously.

III. Low Cost Screened Ground Plane 2 Metal Layer Flexible Circuit Process:

Another process is used to make low cost ground plane flexible circuit using this via forming method and

BNSDOCID: <XP____518622A__I_>

conductive metal paste (screenable . This process is comprised of the steps of:

1) Sputtering a polyimide film on one side with a seed layer of chrome and copper.
2) Plating a flash copper layer on said seed layer.
3) Laminating said photoresist on both sides of said plated film using standard laminating technique with hot rollers.
4) Exposing said photoresist on both sides to ultraviolet light through a photomask, cross linking the exposed portions of the resist.
5) Developing the unexposed portions of the resist with said developing sequence. Normal rinsing with D. I. water and or microetching is also included in this step.
6) Plating copper side of the laminate to desired circuit thickness. This is the first conductive layer.
7) Etching of portions of polyimide film not covered by said resist by said etchant.
8) Etching of said chrome layer by said etchant. This etching exposes certain areas of the circuit on 1st copper layer at the bottom of the holes in the polyimide film, in the bonding window areas, and others.
9) Stripping of said resist on both sides of the laminate in said stripping solution.
10) Screen conductive metal (copper, silver, solder, etc.) paste on PI side into vias and desired area of polymeric film to form a ground plane connected to 1st conductive layer through vias.
11) Baking in oven to sinter or reflow metal paste.
12) Etching of said flash copper on lead side to produce 1st copper layer circuitry.
13) Etching of chrome under flash copper in 1st conductive layer.

In this process the flash etching was done last to provide cantilever leads with support during screen printing and to clean the copper from the oxidation occurred during metal reflow process.

IV. Double Circuit 2 Metal Layer Flexible Circuit Process:

When fine line circuitry is desired on both metal surfaces instead of one side with a ground plane, the above process can be modified to plate the 2nd fine circuitry. This process is comprised of the steps of:

1) Sputtering a polyimide film on one side with a seed layer of chrome and copper.
2) Plating a flash copper layer on said seed layer.

BNSDOCID: <XP____518622A__I_>

3) Laminating said photoresist on both sides of said plated film using standard laminating technique with hot rollers.
4) Exposing said photoresist on both sides to ultraviolet light through a photomask, cross linking the exposed portions of the resist.
5) Developing the unexposed portions of the resist with said developing sequence. Normal rinsing with D. I. water and or microetching is also included in this step.
6) Plating copper side of the laminate to desired circuit thickness. This is the first conductive layer.
7) Etching of portions of polyimide film not covered by said resist by said etchant.
8) Etching of said chrome layer by said etchant. This etching exposes certain areas of the circuit on 1st copper layer at the bottom of holes in polyimide film, in bonding window areas, and others.
9) Stripping of said resist on both sides of the laminate in said stripper.
10) Cleaning of the article with normal cleaning solution, e.g., hydrogen peroxide-sulfuric acid.
11) Baking of the article in hot oven to remove all absorbed water.
12) Sputtering said article with conductive layer of metal such as chrome and copper on polymeric film side.
13) Laminating said photoresist on both sides using standard laminating technique with hot rollers.
14) Exposing said photoresist on both sides to ultraviolet light through a photomask, cross linking the exposed portions of the resist on said 2nd sputtered side to form 2nd side circuitry and flood expose on said 1st copper side.
15) Developing the unexposed portions of the resist with above said developing sequence.
16) Plating said 2nd sputtered side with copper to form the second circuitry layer connected to the first circuitry layer through vias.
17) Stripping of resists on both sides of article with said stripping solution.
18) Etching of said thin flash copper on 1st lead side and sputtered copper on 2nd side using said etchant to produce circuitry of both sides.
19) Etching of chrome under removed copper layers in both sides.

Again, this process needs only one polyimide etching step since vias and windows were etched simultaneously.

BNSDOCID: <XP____518622A__I_>

2244 Research Disclosure
(1995) May, No. 373, Emsworth, GB

V. Plated Ground Plane 2 Metal Layer With Through Holes Flexible Circuit Process:

In another design it is desirable to have through vias (same as on circuit boards) and blind vias as said above, the process can again be modified to accommodate this design. The differences between this process and the said ground plane process are:

a) Only one polyimide etch step is used here.
b) Some holes are milled completely through along with some blind vias.
c) Second conductive layer is plated up to desired pattern instead of etched down.
d) Flash copper on 1st conductive layer is removed first to form through holes, not last as in said ground plane process.

This process is comprised of the steps of:
1) Sputtering a polyimide film on one side with a seed layer of chrome and copper.
2) Plating a flash copper layer on said seed layer.
3) Laminating said photoresist on both sides of said plated film using standard laminating technique with hot rollers.
4) Exposing said photoresist on both sides to ultraviolet light through a photomask, cross linking the exposed portions of the resist.
5) Developing the unexposed portions of the resist with said developing sequence. Normal rinsing with D. I. water and or microetching is also included in this step.
6) Plating copper side of the laminate to desired circuit thickness. This is the first conductive layer.
7) Etching of portions of polyimide film not covered by said resist by said etchant.
8) Stripping of said resist on both sides of the laminate in said stripper.
9) Etching of said chrome layer by said etchant. This etching exposes certain areas of the circuit on 1st copper layer at the bottom of holes in polyimide film, in bonding windows, and other areas.
10) Etching of said flash copper on said 1st conductive layer with said etchant.
11) Etching of sputtered chrome layer under said layer of copper using said etchant. The circuit is now completely defined in 1st copper layer with through holes surrounded by copper rings. The etching of polyimide film was controlled so that portions of said

BNSDOCID: <XP____518622A__I_>

2244 Research Disclosure
(1995) May, No. 373, Emsworth, GB

copper rings are visible and connectable from polyimide side.
12) Cleaning of the article with normal cleaning solution, e.g., hydrogen peroxide-sulfuric acid.
13) Baking of the article in hot oven to remove all absorbed water.
14) Sputtering said article with conductive layer of metal such as chrome and copper on polymeric film side.
15) Laminating said photoresist on both sides using standard laminating technique with hot rollers.
16) Exposing said photoresist on both sides to ultraviolet light through a photomask, cross linking the exposed portions of the resist on said 2nd sputtered side to form 2nd side circuitry.
17) Developing the unexposed portions of the resist with above said developing sequence.
18) Plating said 2nd sputtered side with copper to form the 2nd ground plane connected to the first circuitry layer through vias.
19) Stripping of resists on both sides of article with said stripping solution.
20) Etching of said sputtered copper layer on said 2nd copper side to produce circuitry using said etchant.
21) Etching of chrome under sputtered copper layer in 2nd side.

VI. 3 Metal Layer Flexible Circuit Process:

The 2 metal layer flexible circuit process mentioned above can be extended further to get a 3 metal layer circuit. The third layer of metal is sometime necessary to enhance and optimize electrical performance. The third copper layer was formed by coating a layer on polyimide on the first layer of circuitry, then sputtering and plating of copper on coated polyimide. The process is comprised of the steps of:

1) Sputtering a seed layer of chrome and copper on one side of polyimide.
2) Plating a flash copper layer on said seed layer.
3) Laminating said resist on both sides.
4) Exposing both sides to U.V. light through photomasks.
5) Developing both sides with said developing sequence.
6) Plating copper to desired thickness to form circuitry.
7) Etching of polyimide in unexposed areas to make holes.
8) Stripping of resists on both sides using said stripper.
9) Etching of sputtered chrome in bottom of etched holes.
10) Baking of part in oven to remove all absorbed water.
11) Sputtering another seed layer of chrome and copper on the other side of polyimide.

BNSDOCID: <XP____516622A__I_>

12) Plating of copper on recently sputtered surface to form ground plane.
13) Laminate said resist on ground plane side.
14) Etching of flash and sputtered copper on lead side.
15) Etching of chrome on lead side.
16) Plating of black chrome on lead side
17) Stripping of said resist.
18) Baking of part in oven to remove water.
19) Coating and drying of liquid polyimide on said lead side.
20) Baking of part to imidize coated polyimide.
21) Laminating of resist on said coated polyimide.
22) Exposing of hole pattern on said resist.
23) Developing hole pattern.
24) Etching of hole pattern in coated polyimide.
25) Stripping of said resist on top of coated polyimide.
26) Baking of part to remove water.
27) Sputtering the third seed layer on patterned, coated polyimide.
28) Plating of the third copper layer on said seed layer.
29) Laminating of resists on both sides of the laminate.
30) Exposing of patterns on both side.
31) Developing of resists on both sides.
32) Etching of the two copper layers on the outside of the laminate.
33) Etching of the two sputtered chrome layers.
34) Etching of original polyimide film and coated polyimide simultaneously.
35) Stripping of resists on both sides of the laminate.

In the two copper plating steps, step #12, and 28, the copper surface on the other side each case must be protected from also plating by masking or protecting with mechanical means, tape, or photoresist itself. This process is lengthy and more suitable for sheet or rigid form than roll to roll form. Lengthy process like the above is however common in semiconductor industry for forming multilayer circuitry.

vii. Processes for very fine line, multi-metal layer circuits

This process is necessary if through-hole vias are required in concert with blind vias in a fine line multi-metal flex circuit construction with cantilevered leads. In this case, the width of the cantilevered leads in the inner lead region of the circuit are so narrow that the trauma from processing using some the previously described methods causes damage to the leads. The following process prevents this lead damage because it allows the through-hole vias to

be formed during the first flash etching step while preserving the flash copper layer in the inner lead region until the final steps in the process. The process is comprised of the following steps:

1) Sputtering a seed layer of chrome and copper on one side of polyimide.
2) Plating a flash copper layer on said seed layer.
3) Laminating said resist on both sides.
4) Exposing both sides to U.V. light through photomasks.
5) Developing both sides with said developing sequence.
6) Plating copper to desired thickness to form circuitry.
7) Etching of polyimide in unexposed areas to make holes.
8) Stripping of resists on both sides using said stripper.
9) Etching of sputtered chrome in bottom of etched holes.
10) Laminating said resist on both sides.
11) Exposing one side (the ground plane side or less complex circuit side) with a pattern such that the regions of the circuit containing the through-holes. Flood exposing the opposite side of the circuit.
12) Developing the unexposed portions of the resist with said developing sequence.
13) Etching the flash copper layer in the regions of the circuit not protected with photoresist with said etchant.
14) Cleaning of the article with normal cleaning solution, e.g., hydrogen peroxide-sulfuric acid.
15) Baking of the article in hot oven to remove all absorbed water.
16) Sputtering said article with conductive layer of metal such as chrome and copper on polymeric film side.
17) Laminating said photoresist on both sides using standard laminating technique with hot rollers.
18) Exposing said photoresist on both sides to ultraviolet light through a photomask, cross linking the exposed portions of the resist on said 2nd sputtered side to form 2nd side circuitry.
19) Developing the unexposed portions of the resist with above said developing sequence.
20) Plating said 2nd sputtered side with copper to form the 2nd ground plane connected to the first circuitry layer through vias.
21) Stripping of resists on both sides of article with said stripping solution.
22) Etching of said sputtered copper layer on said 2nd copper side to produce circuitry using said etchant.
23) Etching of chrome under sputtered copper layer in 2nd
24) side.

Disclosed Anonymously
37306